REMARKS

Present Status of Application

The Office Action dated August 24, 2005, rejected claims 7-15 under 35 USC§102(e) as being anticipated by Noguchi et al. (US Publication No. 2003/0042558 A1).

Claim 7 has been amended for providing more descriptions. No new matter has been added to the application by the amendments made to the specification, claims and drawings. This Amendment is promptly filed to place the above-captioned case in condition for allowance. After entering the amendments and considering the following discussions, a notice of allowance is respectfully solicited.

Discussion for 35 USC§102 rejections

Claims 7-15 were rejected under 35 USC§102(e) as being anticipated by Noguchi et al. (US Publication No. 2003/0042558 A1).

The Applicant has carefully considered the remarks set forth in the Office Action.

Claim 7 has been amended to provide more descriptions for clarification purposes, according to the present invention. Supporting grounds for this amendment can be found at least in paragraphs [0027]-[0028] of the specification. Applicant respectfully asserts that claim 7 is patentably distinct from the prior art structures.

As amended, independent claim 7 recites:

7. A multi-level memory cell, comprising:
a substrate;
a gate disposed over the substrate;
a source region and a drain region configured in the substrate on each side of the gate;
a tunneling dielectric layer disposed between the gate and the substrate;
a charge-trapping layer disposed between the tunneling dielectric layer and the gate; and
*a top dielectric layer disposed between the charge-trapping layer and the gate, **wherein the top dielectric layer has at least two portions from the source region to the drain region, and the portion adjacent to the source region has a different thickness to that of the portion adjacent to the drain region, and wherein the tunneling dielectric layer has substantially a same thickness from the source region to the drain region.***.

The Office Action considered Noguchi's layers 4, 3 and 2 being respectively comparable to the top dielectric layer, charge-trapping layer and the tunneling dielectric layer of this application. Applicant respectfully disagrees with this consideration.

Noguchi et al. merely discloses a non-volatile memory cell with the three-layered ONO gate insulation layer. The gate insulation layer includes a first insulation layer 2, a charge accumulating layer 3 and a second insulation layer 4. The feature of the structure as suggested by Noguchi lies in that the thickness (t_{ox2}) of the flat portion of the second insulation layer 4 is more than 5 nm. As mentioned by Noguchi, ".....in order to prevent spreading of the threshold value due to deflection of electric field applied at the time of write in and erasing, each of the thickness of the respective layers 2, 3, 4 constituting the gate insulation film is desired to be equal from a boundary between the semiconductor region 1 and the source region 9 to a boundary between the semiconductor region 1 and

the drain region 10." (paragraph [0050]).

Clearly, as shown in Noguchi's Fig. 1, the second insulation layer 4 below the gate electrode 5 and between the source/drain boundaries is **flat** and of an equal thickness.

Obviously, Noguchi fails to disclose the top dielectric layer has at least two portions from the source region to the drain region, and the portion adjacent to the source region has a different thickness to that of the portion adjacent to the drain region, as recited in claim 7.

In Noguchi's design, the second insulation layer 4 is designed to have a thick flat portion (more than 5 nm) below the gate electrode 5 for preventing spreading of the threshold value due to deflection of electric field. Hence, Noguchi's memory cell can only store one single bit for the unvarying electric field.

Contrarily, in the design of the present invention, due to the top dielectric layer having at least two portions with different thicknesses, charges will be trapped into the portion where the top dielectric layer has a thinner thickness first and then trapped into other portions which have thicker thickness sequentially. Therefore, a single memory cell of this invention can register multiple bits.

Accordingly, the structure of the present invention is patentably distinct from the prior art reference Noguchi. As a result, Noguchi did not anticipate the present invention as suggested by the Office Action, to arrive at the present invention as recited in

independent claim 7. For at least the foregoing reasons, all pending claims patently define over the cited reference and should be allowed.

Consequently, reconsideration and withdrawal of these 102 rejections are respectfully requested.

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CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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